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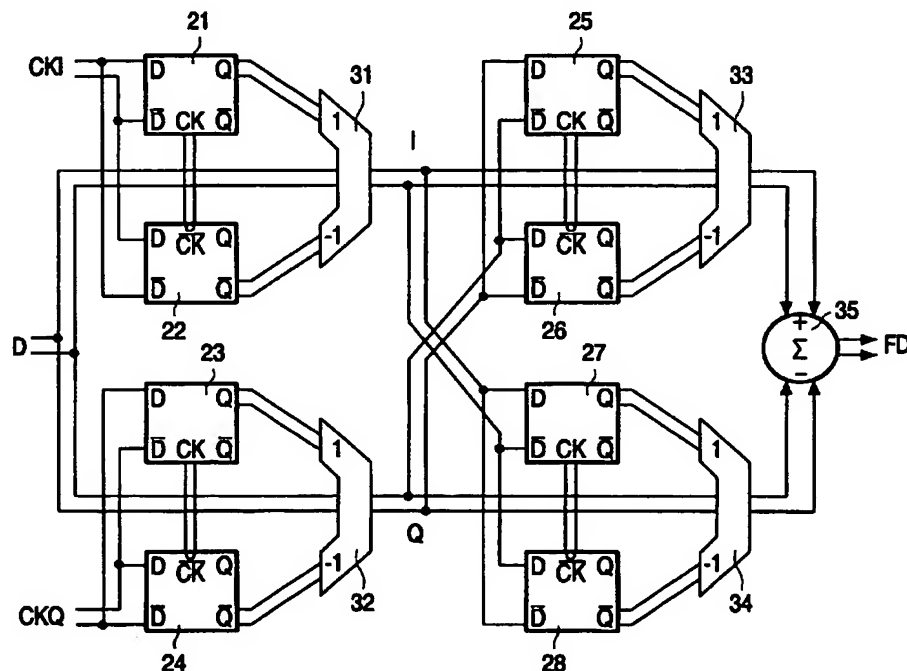
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(54) Title: PLL WITH BALANCED QUADRICORRELATOR



(57) Abstract: A Phase Locked Loop (1) comprising a frequency detector (10) including a balanced quadricorrelator (2), the loop (1) being characterized in that the quadricorrelator (2) comprises double edge clocked bi-stable circuits (21, 22, 23, 24, 25, 26, 27, 28) coupled to multiplexers (31, 32, 33, 34) being controlled by a signal having the same bitrate as the incoming D signal (D).

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**Declaration under Rule 4.17:**

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU,

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# INTERNATIONAL SEARCH REPORT

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**A. CLASSIFICATION OF SUBJECT MATTER**  
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According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)  
EPO-Internal, PAJ, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	SAVOJ J ET AL: "Design of half-rate clock and data recovery circuits for optical communication systems" PROCEEDINGS OF THE 38TH. ANNUAL DESIGN AUTOMATION CONFERENCE. (DAC). LAS VEGAS, NV, JUNE 18 - 22, 2001, PROCEEDINGS OF THE DESIGN AUTOMATION CONFERENCE, NEW YORK, NY: ACM, US, vol. CONF. 38, 18 June 2001 (2001-06-18), pages 121-126, XP010552368 ISBN: 1-58113-297-2 the whole document --- -/--	1-7

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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## INTERNATIONAL SEARCH REPORT

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CHAN GEUN YOON ET AL: "DIGITAL LOGIC IMPLEMENTATION OF THE QUADRICORRELATORS FOR FREQUENCYDETECTOR" PROCEEDINGS OF THE MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS. LAFAYETTE, AUG. 3 - 5, 1994, NEW YORK, IEEE, US, vol. 2 SYMP. 37, 3 August 1994 (1994-08-03), pages 757-760, XP000531787 ISBN: 0-7803-2429-3 cited in the application the whole document	1-7
Y	US 2002/085657 A1 (BOERSTLER DAVID WILLIAM) 4 July 2002 (2002-07-04) paragraph '0051! - paragraph '0053!; figures 8-12	1-7
A	C.K. KEN YANG: "Timing Recovery" COURSE EE219A LECTURE 17, 'Online! 4 June 2001 (2001-06-04), XP002264983 Retrieved from the Internet: <URL:www.icsl.ucla.edu/{yang/ee219a/ee219a_lect_crc.pdf}> 'retrieved on 2003-12-12! page 9 page 12 -page 13	1-7

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002085657	A1	04-07-2002	NONE